



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,012	07/29/2002	Tajinder Manku	085908-000000US	5886

20350 7590 08/12/2004

TOWNSEND AND TOWNSEND AND CREW, LLP  
TWO EMBARCADERO CENTER  
EIGHTH FLOOR  
SAN FRANCISCO, CA 94111-3834

EXAMINER
----------

JACKSON, BLANE J

ART UNIT	PAPER NUMBER
----------	--------------

2685

DATE MAILED: 08/12/2004

9

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/070,012

Applicant(s)

MANKU ET AL.

Examiner

Blane J Jackson

Art Unit

2685

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22, 25 and 26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10, 13-22, 25 and 26 is/are rejected.
- 7) ☒ Claim(s) 10-12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>7.8</u>   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 13-22, 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ward et al. (U.S. Patent 4,736,390).

As to claims 1 and 21, Ward teaches a radio frequency down-converter and method for reduced local oscillator leakage for demodulating an input signal  $X(t)$  comprising:

A synthesizer for generating mixing signals  $S1$  and  $S2$ , which vary irregularly over time where  $S1 \times S2$  has significant power at the frequency of a local oscillator signal being emulated and neither  $S1$  nor  $S2$  has significant power at the frequency of the local oscillator signal being emulated (figure 2,  $S1$  is PN code modulated LO and  $S2$  is the PN code making them irregular in time, column 6, lines 45-60),

A first mixer coupled to the synthesizer for mixing the input signal  $X(t)$  with the mixing signal  $S1$  to generate an output signal  $X(t)S1$  (figure 2, mixer (30) or figure 4 for quadrature mixer configuration where the first mixer(s) are (44) and (47)), and,

A second mixer coupled to the synthesizer and to the output of the first mixer for mixing the signal  $X(t)S1$  with the mixing signal  $S2$  to generate an output signal  $X(t)S1S2$

(figure 2, first mixer (30) and second mixer (34), column 5, lines 12 to column 6, line 10).

As to claim 2, Ward teaches the synthesizer further comprises:

A synthesizer for generating mixing signals S1 and S2 where  $S1 \times S1 \times S2$  does not have a significant amount of power within the bandwidth of the input signal X(t) at base band (figures 2 and 3A-3E, power removed by HPF after first mixer (30)).

As to claim 13, Ward teaches wherein the synthesizer generates mixing signals S1 and S2 that can change with time in order to reduce errors (figures 2-4, the PN code comprising S2 and the PN code modulated LO of S1 provides changes with respect to time and used to spread / de-spread the input signal is one of two circuit effects to reduce the DC offsets, column 5, lines 12-14 and column 6, lines 11-26).

As to claim 14, Ward teaches a filter for removing unwanted signal components for the  $X(t)S1$  signal (figures 2 or 4, a low/ high pass filter (35), (36) or (45), column 5, lines 56-66).

As to claims 15-17, Ward teaches the mixing signals S1 and S2 are based on a pseudo-random noise generator, random, pseudo random and irregular (figure 2: PN Code Generator (33), column 5, lines 19-23 and column 7, lines 2-11).

As to claims 18 and 19, Ward teaches double balanced mixers with inherent port isolation since port isolation is necessary to reduce DC offsets (column 4, line 63 to column 5, line 4). It is well known in the art that Gilbert cell mixers require the local oscillator input to be a digital or square differential waveform to properly switch the modulating transistors on and off for expected performance.

As to claim 20, Ward teaches a local oscillator or frequency synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency (figures 1-4, internal frequency synthesis control fundamental to synthesizers to achieve the system required tuning control and output, column 4, lines 7-10, column 5, lines 16-19).

As to claim 22, Ward teaches an integrated circuit comprising the radio frequency down converter of claim 1 (column 2, lines 14-25, column 4, lines 43-52).

As to claims 25 and 26, Ward teaches the radio frequency down converter of claim 1 where the synthesizer uses different patterns or a single time base to generate both mixing signals S1 and S2 (figure 2, column 7, lines 2-11, the PN Code Generator (33)).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ward et al. (U.S. Patent 4,736,390) with a view to Sevenhans et al. (U.S. Patent 5,422,889).

As to claims 3-9 with respect to claim 2, Ward teaches the radio frequency down converter of claim 2 further comprising circuits to minimize DC offset (figure 2 and 3D, the high pass filter (35) and low pass filter (36) reject most offset power, column 5, line 56 to column 6, line 26) but does not teach a DC offset correction circuit comprising a DC source having a DC output.

Sevenhans teaches a DC offset correction circuit for a direct conversion receiver including:

A DC source having a DC output (figure 1, signals in and out of summer SB of the Offset Correction Circuit (OCC)),

A summer for adding the DC output to an output of one of the mixers (figure 1, an offset correction circuit with summer SB at the output of both the I and Q base band mixers, column 7, line 36 to column 8, line 8),

A closed loop error correction circuit that comprises an error level measurement circuit and a time varying signal modification circuit for modifying a parameter of one of the mixing signals S1 and S2 to minimize the error level (figure 1, the offset correction

circuit (OCC), column 8, line 66 to column 9, line 20, column 10, line 59 to column 11, line 8),

The error level measurement circuit comprises a power measurement (figure 1, the OCC: power, identified through the input X1 to an ADC, column 11, lines 9-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to upgrade Ward with the offset correction circuit of Sevenhans to accurately cancel rather than simply suppress the causes of DC offset common to direct conversion receivers.

#### ***Allowable Subject Matter***

5. Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Grandfield (U.S. Patent 5,448,772) discloses a stacked double balanced mixer circuit based on the Gilbert Cell. Pace et al. (U.S. Patent 5,471,665) discloses a differential DC offset compensation circuit for a direct conversion receiver.

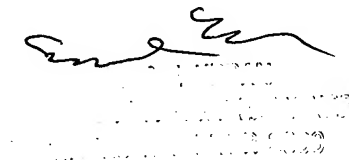
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J Jackson whose telephone number is (703) 305-

5291. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BJJ

A handwritten signature in black ink is written over a rectangular official stamp. The stamp contains several lines of small, mostly illegible text, likely a date and time stamp from a government office.